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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,673	09/30/2004	Chyh-Yih Chang	13714-US-PA	5672

31561 7590 05/02/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

FORDE, REMMON R

ART UNIT PAPER NUMBER

2826

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/711,673

Applicant(s)

CHANG ET AL.

Examiner

Remmon R. Fordé

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/30/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Herbert.

Regarding claims 1, 11, 15 and 16, referencing Figure 1B, Herbert discloses a high voltage device provided with: a first type substrate (29); a first type epitaxial silicon layer (26) disposed in the first type substrate; a first type well (24) disposed in the first type epitaxial silicon layer; a second type well (23 & 28) disposed in the first type epitaxial silicon layer, wherein the second type well comprises a second type lightly doped region (23) and a second type heavily doped region (28), the second type lightly doped region (23) is located next to the first type well (24) and the second heavily doped region (28) is located underneath a portion of the first type well (24) and the second type lightly doped region (23); a gate structure (21) disposed on a portion of the first type well (24) and the second type lightly doped region (23); a second type first doped region (27) and a second type second doped region (22) disposed in the second type lightly doped region (23) and the first type well (24) on each side of the gate structure (21) respectively; a first isolation structure (25) disposed in the second type lightly doped region (23) and between the gate structure (21) and the second type first

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doped region (27); and a first type doped region (19) disposed in the first type well (24) and adjacent to the second type second doped region (22). (Column 1, line 62 – Column 2, line 16.)

Regarding claims 2 and 3, referencing Figure 1B, Herbert further discloses that the second type lightly doped region (23), the first type well (24) and the second type second doped region (22) together constitute a parasitic bipolar transistor, and the second type heavily doped region (28), the first type well (24) and the second type second doped region (22) together constitute another parasitic bipolar transistor so that a pulse current entering from the second type first doped region (27) is able to channel away through the second type second doped region (22) after passing through the two parasitic bipolar transistors. (Column 1, line 62 – Column 2, line 16.)

Regarding claims 4, 5, 12 and 13, referencing Figure 1B, Herbert further discloses a second isolation structure made of a field oxide isolation structure. (Column 1, line 62 – Column 2, line 16.)

Regarding claims 6 and 14, referencing Figure 1B, Herbert further discloses that the first isolation structure (25) is a field oxide isolation structure.

Regarding claims 7 and 17, referencing Figure 1B, Herbert further discloses that the second type first doped region (27), the second type lightly doped region (23) and the second type heavily doped region (28) together serves as a drain and the second type second doped region (22) serves as a source. (Column 1, line 62 – Column 2, line 16.)

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Regarding claims 8 and 18, referencing Figure 1B, Herbert further discloses that the second type lightly doped region (23) comprises a high voltage second type well.

Regarding claims 9 and 19, referencing Figure 1B, Herbert further discloses that the second type heavily doped region (28) comprises a second type buried layer.

Regarding claims 10 and 20, referencing Figure 1B, Herbert further discloses that the first type is a P-type and the second type is an N-type.

Contact Information


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Remmon R. Fordé



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